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Selective Plating for Junction Delineation in Silicon Nanowires

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ABSTRACT

The in situ growth of p–n junctions in silicon nanowires enables the fabrication of a variety of nanoscale electronic devices. We have developed a method for selective coating of Au onto n-type segments of silicon nanowire p–n junctions. Selective plating allows for quick verification of the position of p–n junctions along the nanowire using electron microscopy and allows for measurement of segment length.

Modulation-doped silicon nanowires have been synthesized successfully by varying dopant concentration or dopant type during growth and have been incorporated into electronic devices successfully.[1−3] To better understand the devices, it is valuable to verify the dopant distributions along the wires. However, difficulties have been encountered in characterizing the targeted homojunctions for two reasons. One is that the dopant incorporation does not introduce any obvious crystallographic structure change across the junction that is visible by electron microscopy. Second, the low dopant concentration is not detectable by conventional electron spectroscopy methods (e.g., energy-dispersive spectroscopy). Therefore, special efforts have been made to characterize the modulated silicon nanowires (SiNWs) by first integrating them into devices so that a bias can be applied across the wire and then mapping the doped segments using scanning-gate microscopy or electrostatic-force microscopy.[1−3] Here, we present an electrode-free selective-plating method for junction delineation of modulation-doped multiple p−n junction SiNWs. This allows us to differentiate p- and n-type sections quickly by electron microscopy.

The gold-plating method involves the illumination of p−n junctions to generate carriers necessary for selective electroless plating from a first bath, followed by use of an autocatalytic Au plating bath that plates only on the Au deposited by the first bath. Junction delineation using similar plating methods has been demonstrated on planar silicon devices but have been limited by its resolution.[4,5] These ideas have been extended to plate the n-type regions of silicon nanowire p−n junctions. Because Au is used as the catalyst for vapor−liquid−solid (VLS) growth, it should also be possible to grow NWs from a predetermined location along a wire using the approach developed in this work for selective placement of the Au on the nanowire.

Modulation-doped SiNWs with p−n junctions along their axes were fabricated in a low-pressure, hot-wall chemical-vapor deposition (LPCVD) reactor at 500 °C and 13 Torr via the vapor−liquid−solid (VLS) growth technique. The SiNWs were grown on thin layers of SiO_2 on a Si substrate with a 1-nm Au film as the catalyst. A 10% mixture of SiH_4 in H_2 was used as the Si precursor gas. Silicon nanowires grown in the same LPCVD system without the addition of dopant sources were determined to be p-type with a resistivity on the order of 10^4-10^5 Ω·cm using gated four-point current−voltage measurements on individual SiNWs,[6] and the p-type segments in our NWs were grown with no dopant precursor gas. To intentionally dope segments n-type, phosphine (500 ppm in H_2) was added to the inlet gas mixture. Guided by studies of SiNWs previously grown in the same reactor,[7] a PH_3:SiH_4 ratio of 2×10^{-3} was used to produce heavily doped segments ($\rho = 5 \times 10^{-3}$ Ω·cm) with lengths from <100 nm to 1 μm. The n+ segments were separated by unintentionally doped p-type segments >1 μm in length. The total flow rate of gases through the reactor was held constant at 100 sccm.

After nanowire growth, wafers with SiNWs still attached were dipped in 10:1 buffered oxide etch for a time sufficient to remove any oxide on the wires (1−5 min). Samples were rinsed in deionized (DI) water, then blown dry with N_2 gas, immediately transferred to Oratemp 24 solution (a gold cyanide electroplating solution by Technic), and heated to 35 °C. This commercial plating bath is designed for electrodeposition of films when a potential is applied to the sample, but here we have used it in a different manner. Wafers were submerged to a depth of about 0.5 cm below

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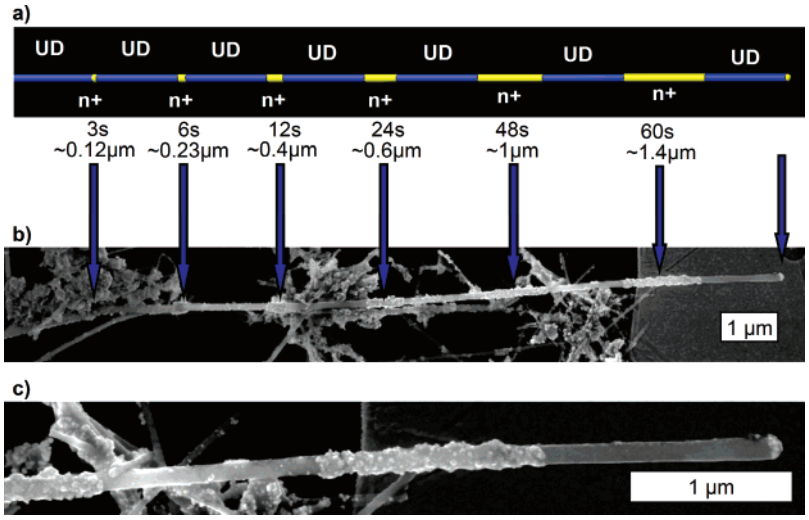

Figure 1. (a) Schematic of modulation-doped silicon nanowire with n+ segments ranging from 1.4 to 0.12 μm. (b) Secondary electron FESEM image of nanowire with gold plated on the n+ segments. (c) Increased magnification image of 1.4 μm segment.

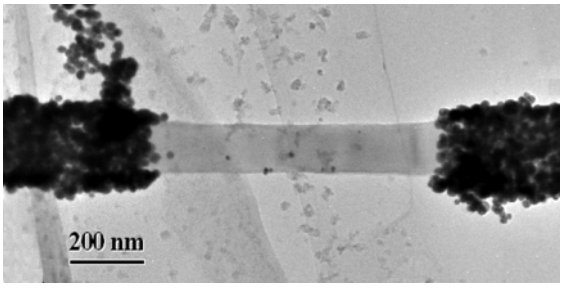

Figure 2. TEM micrograph showing nanoparticle morphology of gold plated on n+ segments.

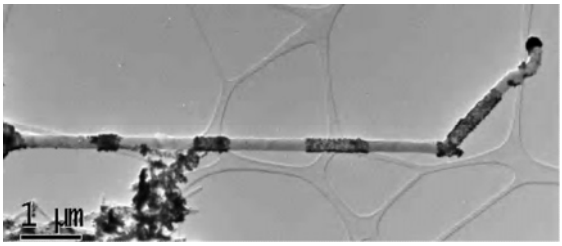

Figure 3. TEM micrograph of one of the modulation-doped silicon nanowires used to make measurements of plated n+ junction lengths.

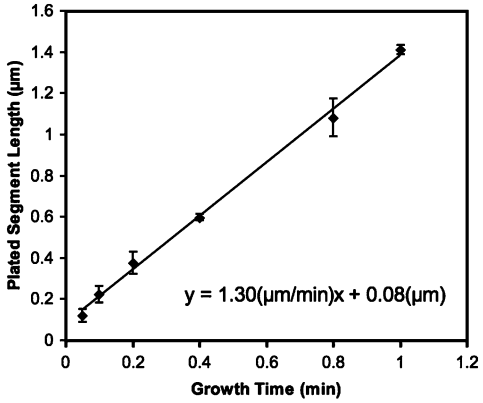

Figure 4. Length of gold-plated segment plotted vs growth time of n+ segments in the silicon nanowires.

the surface of the solution and illuminated under a 12 V 100 W tungsten-halogen lamp at 10 VAC for 6 min to accomplish a photoenhanced electroless seeding of Au on the n-type segments of the SiNWs. The illumination was required to plate gold during this step, and no gold is deposited in the dark. Samples were then rinsed and soaked in DI water for 10 min before being blown dry with nitrogen.

The Au deposited in the previous step was used to selectively catalyze the plating of additional Au by placing the samples into an autocatalytic gold potassium cyanide electroless plating solution at 70 °C.[8] This solution consists of 250 mL of deionized water, 2.8 g of KOH, 1.63 g of KCN, 1.44 g of $KAu(CN)_2$, and 2.9 g of KBH_4. Immersion times of 5 s were sufficient, and no additional illumination was required for this step. Again, samples were rinsed in DI water and blown dry. Following plating, the wires were released from the substrate used for growth using ultrasonic agitation and then dispersed onto a lacey carbon transmission electron microscopy (TEM) grid or Si wafer.

The selectivity of the plating was characterized using field-emission scanning electron microscopy (FESEM) and transmission electron microscopy (TEM). The FESEM micrograph shown in Figure 1 confirms our ability to plate Au selectively on the n-type segments as short as 100 nm. The plated Au consists of many nanoparticles approximately 10 nm in diameter, as shown in the TEM micrograph in Figure 2. Micrographs like the one in Figure 3 were used to measure plated segment lengths, which are plotted in Figure 4 versus time of growth of the n-type segment. Fourteen measurements of the six segment lengths were made, and the standard deviation of the measurements for each segment length is plotted as an error bar. The data can be fit to a straight line with an intercept of 80 nm on the segment-length axis and a slope of 1.3 μm/min. The slope of the line indicates that the growth rate of the n-type segments is 1.3 μm/min, which is similar to the growth rate of our nominally undoped silicon nanowires reported previously.[9] The positive intercept suggests that there is either lateral growth of the Au from the

n-type segment encroaching onto the p-type segments by 40 nm on each side of the junction or that the junction is non-abrupt between the n-type and p-type segments. We would otherwise expect the line to go through the origin.

Additional wires without junctions were also plated to provide insight into the Au deposition mechanism. The n-type wires grown with a PH_3:SiH_4 ratio of 2×10^{-3} had a nonuniform gold coating after plating, less complete than that on the n-type segments in the p−n SiNWs with p−n junctions. Furthermore, the unintentionally-doped p-type wires had no significant gold coating after plating. This, in combination with the requirement for illumination of the wires in the first bath, indicates that the illuminated p−n junction is necessary for uniform plating.

In conclusion, we have shown how to selectively plate gold on the n-type regions of modulation-doped silicon nanowires for junction delineation. The ability to electrolessly deposit metal on segments of nanowires could also facilitate electrical contact formation. Other foreseen uses include the ability to grow more-complicated structures by placement of the gold catalyst at predetermined locations along a nanowire.

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